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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,573	05/03/2002	Ho-Ming Tong	8385-US-PA	9758

31561 7590 02/24/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
EDMONDSON, LYNNE RENEE	
ART UNIT	**PAPER NUMBER**
1725	

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,573	TONG ET AL.	
	Examiner	Art Unit	
	Lynne Edmondson	1725	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33 and 35-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33,35-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 43 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 43 is a duplicate of claim 41.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 4-9, 14-16, 18-23, 28-33, 35, 36 and 41-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Honda (US 2002/0064935 A1).

Honda teaches a method of forming bumps on a silicon wafer having an active surface with a passivation layer (13) and a plurality of bonding pads (12), the method comprising the steps of forming an under bump metallurgy comprising an adhesion

layer (21) comprising Ti or Cr (paragraphs 36 and 40), forming a barrier layer (22, Cu paragraphs 41) over the adhesion layer, forming a wettable layer (24, Cu or Au paragraph 48) over the barrier layer and forming a photoresist (27) over the wettable layer, removing portions of the photoresist and metal layers as is conventional in the art (paragraphs 42-44), attaching a plurality of first Cu or solder blocks (28) to the under bump metallurgy by wire bonding (paragraph 45 and figures 2N and 3A), planarizing the first solder blocks by polishing which includes application of pressure (paragraph 47) and attaching a second plurality of Pb:Sn or Sn:Ag solder blocks (25, paragraphs 48 and 49 and figures 2P and 2Q) by reflow bonding which typically occurs at a temperature above the alloying temperature of the solder. See also Honda claim 22.

4. Claims 14-24, 26, 28-33, 35-37, 39 and 42 are rejected under 35 U.S.C. 102(e) as being anticipated by Chakravorty (USPN 6350668 B1).

Chakravorty teaches a method of forming bumps on a silicon wafer having an active surface with a passivation layer (305) and a plurality of bonding pads (304), the method comprising the steps of forming an under bump metallurgy (307,310) comprising multiple layers of Al, Cr, Ni and combinations of these metals as well as combinations of Cr and Cu (col 8 line s40-45 and col 9 lines 31-36) and forming a photoresist (308) over the wettable layer, removing the photoresist as is conventional in the art (col 8 lines 38-62), attaching a plurality of first Pb:Sn solder blocks (bumps 311-1) to the under bump metallurgy (col 8 line 63 – col 9 line 12) by conventional wire bond bumping (col 9 lines 20-36), planarizing the bumps by polishing (col 11 lines 7-25)

which includes pressing and attaching a second plurality of Pb:Sn solder blocks (314) by reflow bonding (col 11 lines 26-40) which typically occurs at a temperature above the alloying temperature of the solder. See also Chakravorty claims 3-7.

5. Claims 28-33, 35 and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Fang (US 2003/0099767 A1).

Fang teaches a method of forming bumps on a silicon wafer wherein the active surface has a an under bump metallurgy (UBM), attaching a first solder block (212) to an upper surface of the UBM by bonding, planarizing (grinding) the first solder block (paragraph 14) and attaching a second solder block (264) to the upper surface of the first solder block by bonding. Bumps are planarized by polishing (grinding) which uses pressure (paragraphs 26-27). Bumps are bonded by reflow (paragraphs 30- 34). The solder blocks are made of Sn:Pb solders (paragraph 32). See also Fang claims 1-3, 6-9 and 12-15.

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Honda (US 2002/0064935 A1) in view of Agarwala et al. (USPN 5251806).

Honda teaches a method of forming bumps on a silicon wafer having an active surface with a passivation layer (13) and a plurality of bonding pads (12), the method comprising the steps of forming an under bump metallurgy comprising an adhesion layer (21) comprising Ti or Cr (paragraphs 36 and 40), forming a barrier layer (22, Cu paragraphs 41) over the adhesion layer, forming a wettable layer (24, Cu or Au paragraph 48) over the barrier layer and forming a photoresist (27) over the wettable layer, removing portions of the photoresist and metal layers as is conventional in the art (paragraphs 42-44), attaching a plurality of first Cu or solder blocks (28) to the under bump metallurgy by wire bonding (paragraph 45 and figures 2N and 3A), planarizing the first solder blocks by polishing which includes application of pressure (paragraph 47) and attaching a second plurality of Pb:Sn or Sn:Ag solder blocks (25, paragraphs 48 and 49 and figures 2P and 2Q) by reflow bonding which typically occurs at a temperature above the alloying temperature of the solder. Although, Cr and Cu layers are taught, there is no disclosure of a Cu-Cr layer.

Agarwala teaches bonding of wafer bumps with UBM comprising a Cu-Cr layer as a wettable layer col 6 lines 42-50, col 9 lines 12-30 and figure 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ conventional UBM materials such as combinations of Cu and Cr to provide good adherence and diffusion characteristics (Honda, paragraph 40).

8. Claims 10-13, 24-27, 29 and 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Honda (US 2002/0064935 A1) in view of Sakurai (USPN 6455785 B1).

Honda teaches a method of forming bumps on a silicon wafer having an active surface with a passivation layer (13) and a plurality of bonding pads (12), the method comprising the steps of forming an under bump metallurgy comprising an adhesion layer (21) comprising Ti or Cr (paragraphs 36 and 40), forming a barrier layer (22, Cu paragraphs 41) over the adhesion layer, forming a wettable layer (24, Cu or Au paragraph 48) over the barrier layer and forming a photoresist (27) over the wettable layer, removing portions of the photoresist and metal layers as is conventional in the art (paragraphs 42-44), attaching a plurality of first Cu or solder blocks (28) to the under bump metallurgy by wire bonding (paragraph 45 and figures 2N and 3A), planarizing the first solder blocks by polishing which includes application of pressure (paragraph 47) and attaching a second plurality of Pb:Sn or Sn:Ag solder blocks (25, paragraphs 48 and 49 and figures 2P and 2Q) by reflow bonding which typically occurs at a

temperature above the alloying temperature of the solder. However, the wire bonding process is not further disclosed.

Sakurai teaches formation of a solder block on a wafer (20) by providing a conductive wire, heating one end of the wire to form a spherical blob (col 4 lines 30-40) which is pulled toward the wettable layer, pressing, heating and applying ultrasound as is conventional in the art (figures 10, 14 and 24 and col 4 lines 55-65) and detaching the remaining portion of the wire from the spherical blob to form the first solder block (col 5 lines 1-10). Balls are planarized by pressing (figures 17a and 17b and col 5 lines15-24).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ conventional wire bonding techniques to form conductive bumps having uniform heights in a simple and time-effective manner (Honda, col 1 lines 33-40 and col 4 line 64 – col 56 line 4).

9. Claims 25, 27, 38 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty (USPN 6350668 B1) in view of Salmon (US 20030049886 A1).

Chakravorty teaches a method of forming bumps on a silicon wafer having an active surface with a passivation layer (305) and a plurality of bonding pads (304), the method comprising the steps of forming an under bump metallurgy (307,310) comprising multiple layers of Al, Cr, Ni and combinations of these metals as well as combinations of Cr and Cu (col 8 line s40-45 and col 9 lines 31-36) and forming a

photoresist (308) over the wettable layer, removing the photoresist as is conventional in the art (col 8 lines 38-62), attaching a plurality of first Pb:Sn solder blocks (bumps 311-1) to the under bump metallurgy (col 8 line 63 – col 9 line 12) by conventional wire bond bumping (col 9 lines 20-36), planarizing the bumps by polishing (col 11 lines 7-25) which includes pressing and attaching a second plurality of Pb:Sn solder blocks (314) by reflow bonding (col 11 lines 26-40) which typically occurs at a temperature above the alloying temperature of the solder. However, there is no disclosure of ultrasonic vibration.

Salmon teaches formation of a solder block on a wafer by applying ultrasound as is conventional in the art (figure 9A and paragraph 64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply ultrasonic vibration during ball bonding as is conventional to form low inductance, stress-free bumps (Chakravorty, col 3 lines 40-51) in a simple and cost-effective manner (Chakravorty, col 5 lines 63-65).

Response to Arguments

10. Applicant's arguments with respect to claims 1-27 and 37-40 have been considered but are moot in view of the new ground(s) of rejection.

11. Regarding applicant's argument that Fang is not proper prior art it is noted that the instant application comprises a different inventive entity with a common inventor. The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Therefore the 102 rejection of claims 28-33, 35 and 36 as anticipated by Fang stands.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yanagida (USPN 6204558 B1, structure and method), Tan et al. (USPN 6372622 B1), Ho et al. (USPN 6424037), Go (USPN 4912545, reflow as a process where eutectic solder is heated above the alloying temperature) and Lee (US 2003/0089758 A1).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne Edmondson whose telephone number is (571)

272-1172. The examiner can normally be reached on Monday through Thursday from 6:30 a.m. to 5 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Dunn can be reached on (571) 272-1171. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0651.

Lynne Edmondson
Primary Examiner
Art Unit 1725

2/5/04

LRE
February 3, 2004